



AO4447

P-Channel Enhancement Mode Field Effect Transistor

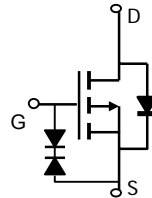
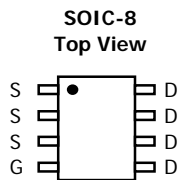
General Description

The AO4447/L uses advanced trench technology to provide excellent $R_{DS(ON)}$, and ultra-low low gate charge. This device is suitable for use as a load switch. The device is ESD protected. AO4447 and AO4447L are electrically identical.
-RoHS Compliant
-AO4447L is Halogen Free

Features

V_{DS} (V) = -30V
 I_D = -15 A (V_{GS} = -10V)
Max $R_{DS(ON)}$ < 7.5m Ω (V_{GS} = -10V)
Max $R_{DS(ON)}$ < 12m Ω (V_{GS} = -4V)
ESD Rating: 4KV HBM

UIS Tested!
Rg, Ciss, Coss, Crss Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{AF}	I_D	$T_A=25^\circ\text{C}$	-15
		$T_A=70^\circ\text{C}$	-13.6
Pulsed Drain Current ^B	I_{DM}	-60	A
Avalanche Current ^G	I_{AR}	40	A
Repetitive avalanche energy L=0.3mH ^G	E_{AR}	240	mJ
Power Dissipation ^A	P_D	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	26	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	50	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	14	24	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -10	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.9	-1.25	-1.6	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-60			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-15A T _J =125°C		6.7 9.4	7.5 12	mΩ
		V _{GS} =-4V, I _D =-13A		9.2	12	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-15A		60		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.69	-1	V
I _S	Maximum Body-Diode Continuous Current				5.5	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		5500	6600	pF
C _{OSS}	Output Capacitance			745		pF
C _{RSS}	Reverse Transfer Capacitance			473		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		3.1	4	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-15A		88.8	120	nC
Q _{g(4.5V)}	Gate Charge			45.2	60	nC
Q _{gs}	Gate Source Charge			10.1		nC
Q _{gd}	Gate Drain Charge			19.4		nC
t _{D(on)}	Turn-On DelayTime			12		ns
t _r	Turn-On Rise Time	V _{GS} =-10V, V _{DS} =-15V, R _L =1.7Ω, R _{GEN} =3Ω		11.5		ns
t _{D(off)}	Turn-Off DelayTime			100		ns
t _f	Turn-Off Fall Time			40		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-15A, di/dt=100A/μs		46.6	60	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-15A, di/dt=100A/μs		67.7		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using <300μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s thermal resistance rating.

G: EAR and IAR ratings are based on low frequency and duty cycles such that T_{J(start)}=25C for each pulse.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

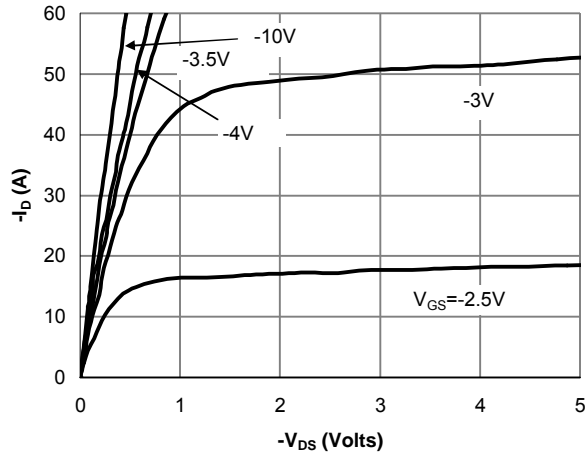


Fig 1: On-Region Characteristics

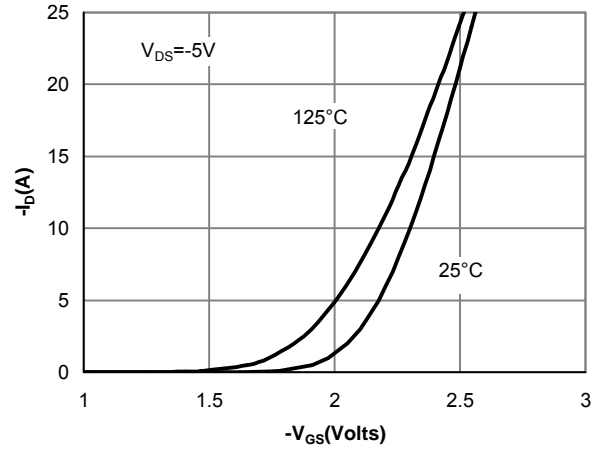


Figure 2: Transfer Characteristics

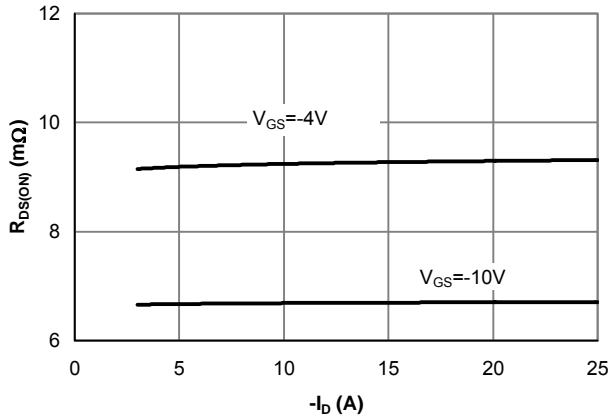


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

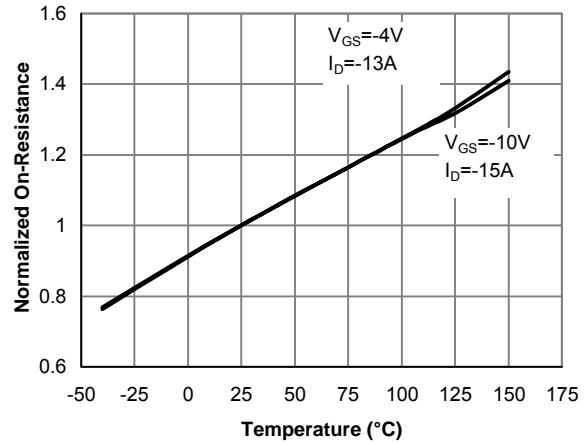


Figure 4: On-Resistance vs. Junction Temperature

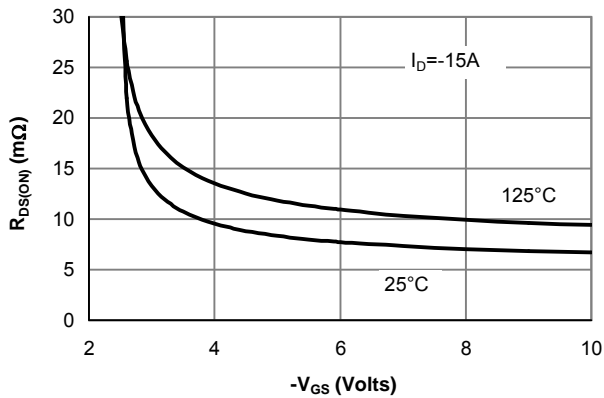


Figure 5: On-Resistance vs. Gate-Source Voltage

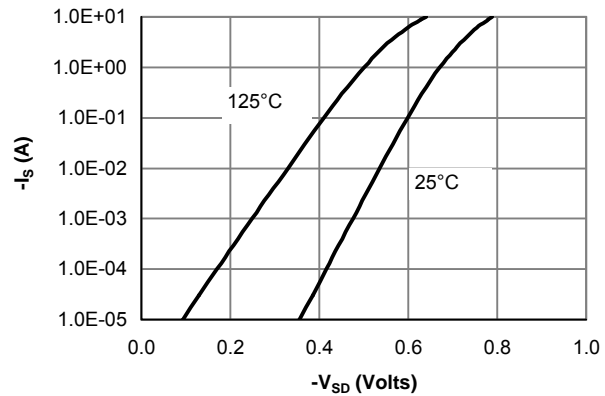


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

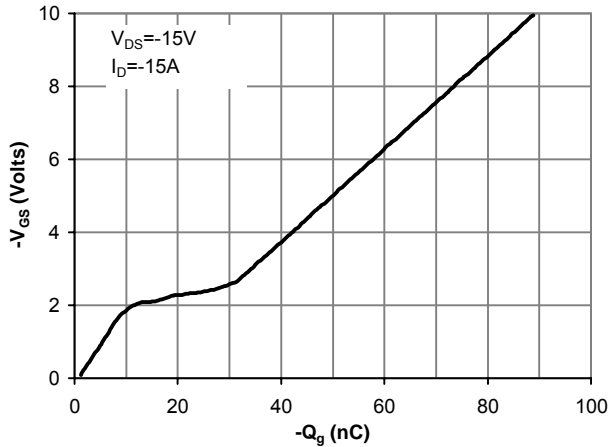


Figure 7: Gate-Charge Characteristics

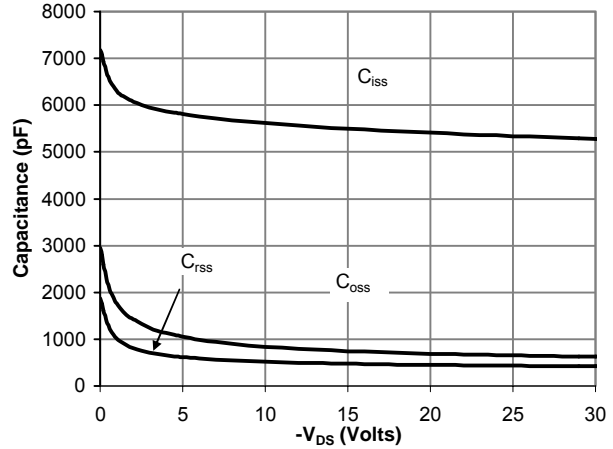


Figure 8: Capacitance Characteristics

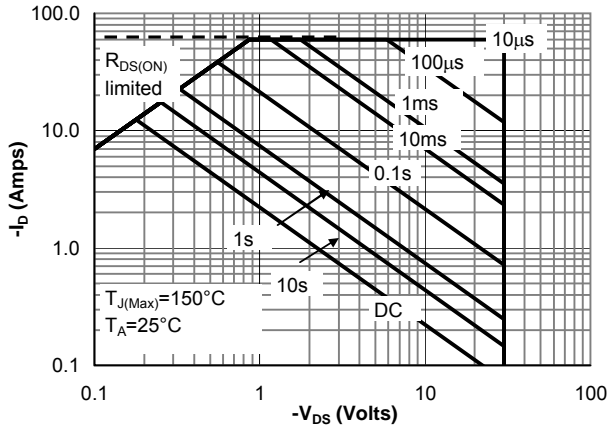


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

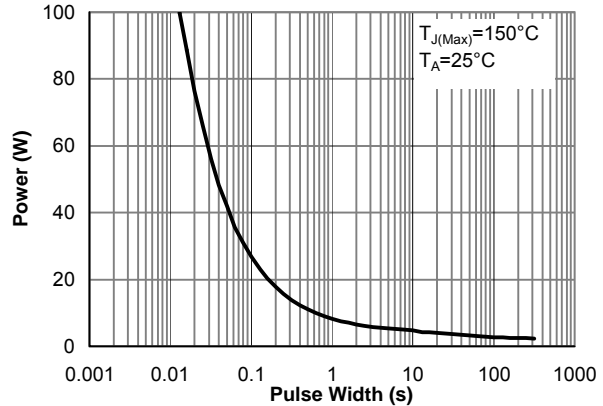


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

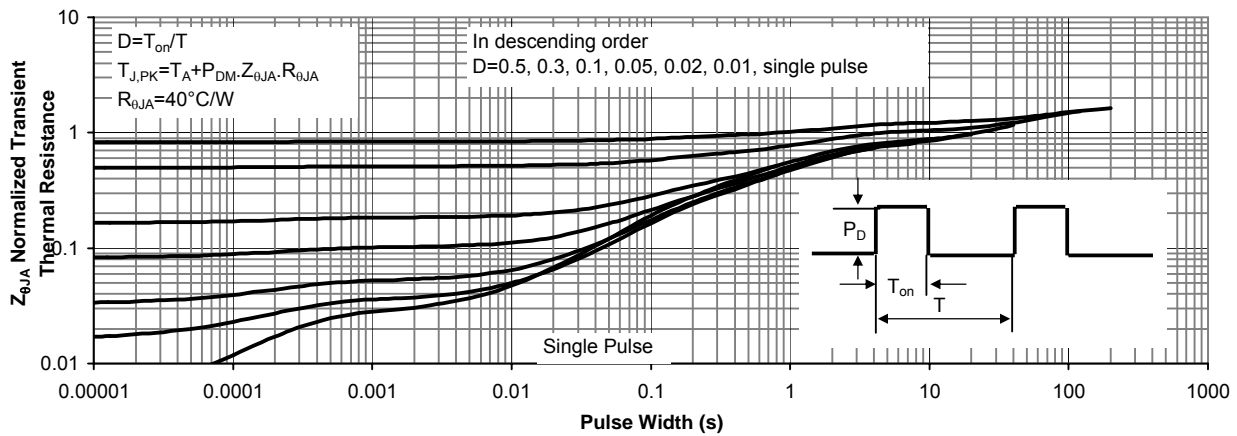


Figure 11: Normalized Maximum Transient Thermal Impedance